

In the claims:

For the Examiner's convenience, all pending claims are presented below with changes shown.

- 1 1. (Previously Presented) A chipset comprising:
2 a graphics accelerator;
3 a memory controller; and
4 a queue mechanism divided to include:
5 a first functional unit block (FUB), coupled to the graphics accelerator at a
6 first physical partition on the chipset die, to perform a first set of functions for the
7 queue mechanism; and
8 a second FUB, coupled to the memory controller at a second physical
9 partition on the chipset die, to perform a second set of functions for the queue
10 mechanism.
- 1 2. (Original) The chipset of claim 1 wherein the queue mechanism further
2 comprises control logic to facilitate an interface between the graphics accelerator and the
3 memory controller.
- 1 3. (Original) The chipset of claim 1 wherein the first FUB is operated based
2 upon a first clock domain and the second FUB is operated according to a second
3 clock domain.

1 4. (Original) The chipset of claim 1 wherein there is unidirectional signaling
2 between the first FUB and the second FUB, such that there will be a strobe and a
3 packet associated with the strobe that flows from the first FUB to the second FUB.

1 5. (Original) The chipset of claim 3 wherein the second FUB comprises
2 storage elements in which to store information that is written into the queue
3 mechanism.

1 6. (Original) The chipset of claim 5 wherein the first FUB comprises:
2 logic associated with a load pointer, wherein the load pointer indicates a location
3 in the storage elements to store information; and
4 match logic.

1 7. (Original) The chipset of claim 6 wherein the second FUB comprises:
2 an unload pointer to indicate a location in the storage elements in which
3 information is to be read from; and
4 clock gating elements to gate the load pointer into the second clock domain.

1 8. (Original) The chipset of claim 7 wherein the match logic compares the load
2 and unload pointer to determine whether information is stored in the queue.

1 9. (Original) The chipset of claim 8 wherein the load pointer is clock crossed to
2 the second clock domain in FUB 1 to save a clock of latency.

1 10. (Original) The chipset of claim 9 wherein the unload pointer is clock crossed
2 to the first clock domain in the second FUB.

1 11. (Original) The chipset of claim 10 wherein data to be stored in the storage
2 elements is directly flopped in the first clock domain within the second FUB.

1 12. (Original) The chipset of claim 10 wherein the clock crossed versions of the
2 load pointer and the unload pointer are used to determine at the second FUB if a
3 command is present.

1 13. (Original) The chipset of claim 12 wherein the availability of space in the
2 storage elements is determined at the match logic by using the load pointer and the clock
3 crossed version of the unload pointer.

1 14. (Previously Presented) A system comprising:
2 a first component;
3 a second component; and
4 a queue mechanism divided to include:
5 a first functional unit block (FUB), coupled to the first component at a first
6 physical partition on an integrated circuit (IC) die, to perform a first set of
7 functions for the queue mechanism; and
8 a second FUB, coupled to the second component at a second physical
9 partition on the IC die, to perform a second set of functions for the queue
10 mechanism.

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1 15. (Original) The system of claim 14 wherein the first FUB is operated based
2 upon a first clock domain and the second FUB is operated according to a second
3 clock domain.

1 16. (Original) The system of claim 15 wherein the second FUB comprises
2 storage elements in which to store information that is written into the queue
3 mechanism.

1 17. (Original) The system of claim 16 wherein the first FUB comprises:
2 logic associated with a load pointer, wherein the load pointer indicates a location
3 in the storage elements to store information; and
4 match logic.

1 18. (Original) The system of claim 17 wherein the second FUB comprises:
2 an unload pointer to indicate a location in the storage elements in which
3 information is to be read from; and
4 clock gating elements to gate the load pointer into the second clock domain.

1 19. (Previously Presented) A queue mechanism comprising:
2 a first functional unit block (FUB), coupled to a first component at a first physical
3 partition on an integrated circuit (IC) die, to perform a first set of functions for the queue
4 mechanism; and
5 a second FUB, coupled to a second component at a second physical partition on
6 the IC die, to perform a second set of functions for the queue mechanism.

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7 control logic to facilitate an interface between the first component and the second
8 component.

1 20. (Original) The queue mechanism of claim 19 wherein the first FUB is
2 operated based upon a first clock domain and the second FUB is operated according
3 to a second clock domain.

1 21. (Original) The queue mechanism of claim 20 wherein the second FUB
2 comprises storage elements in which to store information that is written into the
3 queue mechanism.

1 22. (Original) The queue mechanism of claim 21 wherein the first FUB
2 comprises:
3 logic associated with a load pointer, wherein the load pointer indicates a location
4 in the storage elements to store information; and
5 match logic.

1 23. (Original) The queue mechanism of claim 22 wherein the second FUB
2 comprises:
3 an unload pointer to indicate a location in the storage elements in which
4 information is to be read from; and
5 clock gating elements to gate the load pointer into the second clock domain.

1 24. (Original) The queue mechanism of claim 23 wherein the match logic
2 compares the load and unload pointer to determine whether information is stored in the
3 queue.

1 25. (Original) The queue mechanism of claim 24 wherein the load pointer is
2 clock crossed to the second clock domain in FUB 1 to save a clock of latency.

1 26. (Original) The queue mechanism of claim 25 wherein the unload pointer is
2 clock crossed to the first clock domain in the second FUB.

1 27. (Original) The queue mechanism of claim 26 wherein data to be stored in the
2 storage elements is directly flopped in the first clock domain within the second FUB.

1 28. (Original) The queue mechanism of claim 26 wherein the clock crossed
2 versions of the load pointer and the unload pointer are used to determine at the second
3 FUB if a command is present.

1 29. (Previously Presented) The queue mechanism of claim 28 wherein the
2 availability of space in the storage elements is determine at the match logic by using the
3 load pointer and the clock crossed version of the unload pointer.

1 30. (Previously Presented) A computer system comprising:
2 a memory control hub (MCH) divided into a first physical partition and a second
3 physical partition, having:
4 a graphics accelerator;

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5 a memory controller;
6 a queue mechanism divided to include:
7 a first functional unit block (FUB), coupled to the graphics
8 accelerator at the first physical partition on the MCH, to perform a first set
9 of functions for the queue mechanism; and
10 a second FUB, coupled to the memory controller at the second
11 physical partition on the MCH, to perform a second set of functions for the
12 queue mechanism.

1 31. (Previously Presented) The computer system of claim 30 wherein the queue
2 mechanism further comprises control logic to facilitate an interface between the graphics
3 accelerator and the memory controller.

1 32. (Previously Presented) The computer system of claim 30 wherein the first
2 FUB is operated based upon a first clock domain and the second FUB is operated
3 according to a second clock domain.